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| 10/693,963 | 10/28/2003 | Hidenori Kawata | 117269 | 4561 |

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OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

| EXAMINER | |
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| 2871 | |

DATE MAILED: 08/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/693,963 | KAWATA ET AL. | |
| | Examiner | Art Unit | |
| | Phu Vu | 2871 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on *24 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *7 and 8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

Applicant's arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection.

**Claims 1, 3-6, 9-11, 13-16, 21-24 and 26 are rejected under 35 U.S.C. 102(b) as being obvious over Takashi JP2002-215064 in view of Yasukawa 20020057403 in view of 5978056 Shintani.**

**Regarding claims 1, 2, 13, 18-19 and 25-26,** Takashi teaches an electro-optical device comprising, above a substrate: data lines (fig. 2 element 6a) extending in a first direction; metal scanning lines (3a) extending in a second direction and intersecting the data lines; pixel electrodes (9a) and thin film transistors (fig. 1 3a is the gate of the TFT) disposed so as to correspond to intersection regions of the data lines and the scanning lines; and storage capacitors (fig. 7 element 70) electrically connected to the thin film transistors and the pixel electrodes, wherein the thin film transistors including semiconductor layers (fig. 7 element 1a) having channel regions (1a') which extend in a longitudinal direction and channel adjacent regions(see fig. 8) which further extend from the channel regions in the longitudinal direction, and the scanning lines including light-shielding parts (3b') disposed at sides of the channel regions. Takashi teaches the relay layer as part of a laminated structure (see element 71).

Takashi omits a light shield of relay layer material formed between the data line and pixel electrode. Yasukawa teaches forming a light shield formed of the same material as a relay layer (see [0183] and [0065]) between the data line and pixel

electrode that increases reliability of the TFT by preventing light from entering the channel region [0011]. Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to apply a light shield of the same material as the relay layer between the data line and pixel electrode to increase TFT reliability.

The references omit forming the light shield of a TiN top layer and aluminum lower layer however Shintani discloses a shield layer with an anti-reflection properties formed by TiN and AL layer structure (see column 6 lines 38-47). Therefore, at the time of the invention it would have obvious to one of ordinary skill in the art to apply a TiN and AL light shield to minimize reflection caused by the light shield.

**Regarding claim 3,** the reference teaches the scanning lines including main-body parts (fig. 8 element 3a) extending in a direction which intersects the longitudinal direction and gate electrodes of the thin film transistors overlapped with the channel regions in plan view, and horizontal protrusions (3b') protruding from the main-body parts at the sides of the channel region in the longitudinal direction in plan view and constituting a light-shielding part.

**Regarding claim 4,** the electro-optical device according to claim 3, each of the main-body parts and each of the horizontal protrusions being integrally formed of the same film (see fig. 8).

**Regarding claim 5,** the reference teaches the horizontal protrusions protruding from source and drain sides of the channel regions in plan view (see fig. 8).

**Regarding claim 6,** the reference teaches the thin film transistors including semiconductor layers having channel regions which extend in a longitudinal direction, wherein the electro-optical device, further comprising: upper light-shielding films (fig. 11 element 3a) at least covering the channel regions of the thin film transistors from the upper side, and at least a part of each of the upper light-shielding films being formed in a concave shape in a cross section perpendicular to the longitudinal direction of the channel regions as viewed from the channel regions.

**Regarding claim 9,** the reference teaches the thin film transistors including semiconductor layers having channel regions which extend in the first direction, and the scanning lines including main-line parts (fig. 9 element 3a) including the gate electrodes of the thin film transistors which face the channel regions with the gate insulating films interposed therebetween and extending in the second direction intersecting the first direction in plan view, and vertical (3c) protrusions which protrude downwardly from the main-line parts at positions which are separated from the channel regions by a predetermined distance in the second direction in plan view.

**Regarding claim 10,** the reference teaches an electro-optical device further comprising: above the substrate, lower light-shielding films (fig. 10 element 11a') covering at least the channel regions from the lower sides thereof, the vertical protrusions (3c) contacting the lower light-shielding films at front ends.

**Regarding claim 11,** the reference teaches above the substrate, lower light-shielding films (fig. 9 element 11a) covering at least the channel regions from the lower

sides thereof, the vertical protrusions (3c) not contacting the lower light-shielding films at the front ends.

**Regarding claim 14,** the reference teaches, one of a pair of electrodes constituting each of the storage capacitors (fig. 7 element 70) constituting a part of a capacitive line formed along the second direction, and the capacitive line being made of a multi-layered film including a low-resistive film (300).

**Regarding claim 15,** the reference teaches, the pixel electrodes being electrically connected to other layers of a laminated structure through a titanium simple substance, a tungsten simple substance, a compound of titanium and tungsten, or a stack thereof ([0064]).

**Regarding claim 16**, the reference teaches a laminated structure further including interlayer insulating films provided as bases of the pixel electrodes (fig. 7 elements 42-43), contact holes (85) being formed in the interlayer insulating films to electrically connect the pixel electrodes thereto, and films (300, 71, 75) being formed as at least inside surfaces of the contact holes and lower layers of the pixel electrodes, the films including a titanium simple substance, a tungsten simple substance, a compound of titanium or tungsten, or a stack thereof [0064].

**Regarding claim 20,** the primary reference teaches at least the storage capacitors being made of a light shielding material and constituting a light shielding firm in a laminated structure.

**Regarding claims 21-22,** the reference teaches the light-shielding films disposed in the light-shielding regions, the light-shielding films including metal layers which contain a high-melting-point metal simple substance or metal compounds, and barrier layers which are made of a high-melting-point and oxygen-free metal or metal compounds laminated on at least one surface of the metal layers and the metal layers of the light-shielding films including light-shielding metal layers and light-absorption metal layers, the light-absorption metal layers facing the thin film transistor [(see [0064-0065]). The relay layer is made of polysilicon a light-absorption material and the relay layer, dielectric layer, and capacitor layer are considered to form the multilayer light shield

**Regarding claim 23** the reference teaches each of the metal layers being interposed between the barrier layers when considering a barrier layer to be an oxygen free metal as the references teaches forming the multiple oxygen free metal layers (see [0064-0065]).

**Regarding claim 24**, considering the capacitor electrode to be the light shield (element 300 see [0070]) than the shield layers are set to a fixed electrode.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takashi in view Yasukawa in view of Shintani in view of Masao JP2002-244155.**

**Regarding claim 12,** Takashi teaches the thin film transistors including semiconductor layers having channel regions which extend in the first direction, the scanning lines including the main-line parts including the gate electrodes of the thin film transistors which face the channel regions with the gate insulating films interposed therebetween and extending in the second direction intersecting the first direction in plan view (see claim 9 rejection). The reference fails to teach the main-line parts being disposed inside grooves engraved in the substrate and including inside-groove parts which cover at least a part of the channel regions from the sides thereof. Masao teaches main line parts being disposed inside grooves engraved in the substrate and including inside-groove parts which cover at least a part of the channel region from the sides (fig. 3 10CV )to reduce the difference in electric field where wiring components exist and other regions [0068]. Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to apply an inside-groove part with main line disposed inside the groove parts, which cover a part of the channel region from the sides to reduce the difference in electric field between the regions.

**Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takashi in view of Yasukawa in view of Shintani in view of Shimada US 593085.**

**Regarding claim 17,** Takashi teaches the data line made of aluminum [0002]. The reference fails to teach an electrode of the capacitor to be made of aluminum. Shimada teaches a capacitor electrode made of an an ionically oxidizable material that prevents short circuit between the storage capacitor and the pixel electrode (column 5 lines 55-65). Therefore, at the time of the invention it would have been obvious to one of ordinary skill in the art to use an aluminum storage capacitor to prevent short circuit with the pixel electrode.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phu Vu whose telephone number is (571)-272-1562. The examiner can normally be reached on 8AM-5PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phu Vu
Examiner
AU 2871

ANDREW SCHECHTER
PRIMARY EXAMINER